(12) INTERNATIONAL [redacted]ICATION PUBLISHED UNDER THE PATE[redacted] COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
15 February 2001 (15.02.2001)

PCT

(10) International Publication Number
WO 01/11669 A1

(51) International Patent Classification[7]: H01L 21/28, 21/8238

(21) International Application Number: PCT/EP00/07519

(22) International Filing Date: 2 August 2000 (02.08.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
9910309 9 August 1999 (09.08.1999) FR

(71) Applicants *(for all designated States except US)*: **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL). **STMICROELECTRONICS S.A.** [FR/FR]; 7, avenue Galliéni, F-94250 Gentilly (FR). **FRANCE TELECOM** [FR/FR]; 6, place d'Alleray, F-75015 Paris (FR).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **DE COSTER, Walter, J., A.** [BE/NL]; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **GERRITSEN, Eric** [NL/NL]; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **BASSO, Marie-Therese** [FR/NL]; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: **DUIJVESTIJN, Adrianus, J.**; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

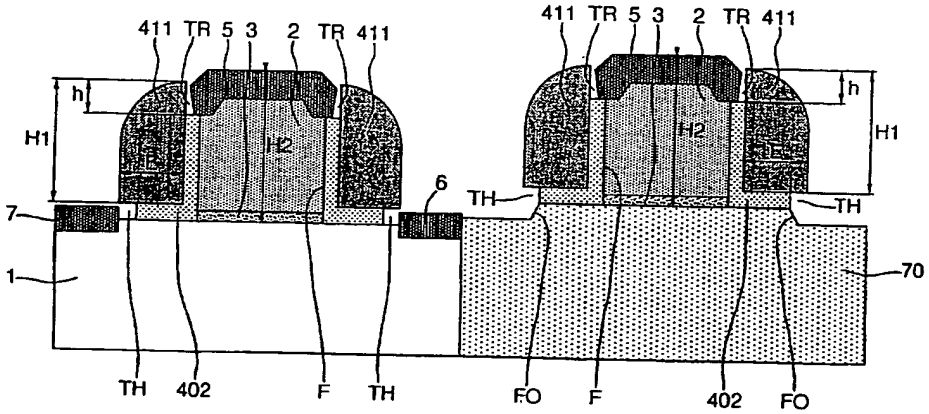
(81) Designated States *(national)*: JP, US.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published:
— *With international search report.*
— *Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SALICIDE PROCESS FOR MOSFET INTEGRATED CIRCUIT



(57) Abstract: The integrated circuit comprises lateral isolation regions formed at the sides of at least one projecting polysilicon region so as to be in contact therewith, said lateral isolation regions each being composed of a smaller isolation layer (402), which is in contact with said projecting region (2), and of a larger isolation layer (411), and it further comprises a zone (5) including a metal silicide situated in the upper part of the polysilicon region (2). Each lateral isolation region comprises a vertical trench (TR) made in the smaller isolation layer (402) between the larger isolation layer (411) and the corresponding side (F) of the projecting region (2), said trench (TR) extending from the top of the larger isolation layer (411) of the corresponding lateral isolation region down to a predetermined depth (h).

WO 01/11669 A1

SALICIDE PROCESS FOR MOSFET INTEGRATED CIRCUIT

The invention relates to the manufacture of an integrated circuit, more particularly to the formation of metal silicide zones on the polysilicon regions forming, for example, the gate regions of the field effect transistors.

In Figure 1, which very diagrammatically shows a field effect transistor in accordance with the prior art the gate of which is covered with a metal silicide 5, reference numeral 1 denotes a semiconductor substrate within which the field effect transistor is formed. As is customary, said field effect transistor comprises a projecting portion of polysilicon 2, which forms the gate region of the transistor, said projecting portion being isolated from the substrate by a gate oxide 3, which typically consists of silicon dioxide.

The transistor also comprises lateral isolation zones or spacers 4, which are provided at the sides of the gate region 2 so as to be in contact therewith. These spacers are customarily composed of two layers, i.e. a smaller isolation layer 40, which is generally composed of an oxide (for example, tetraethyl orthosilicate ($Si(OC_2H_5)_4$); also referred to as TEOS in English), and a larger isolation layer 41, which is generally composed of silicon nitride Si_3N_4. Silicon nitride enables better etching of the spacers while the smaller isolation layer forms a buffer layer against the stresses induced in the underlying silicon by the nitride layer.

The manufacture of the transistor also comprises a stage wherein the source, drain and gate regions of the transistor are subjected to a silicidation process. This silicidation process includes, inter alia, the deposition of a metal, such as titanium or cobalt, which, in combination with silicon, is capable of forming a metal silicide, for example titanium silicide $TiSi_2$. This results in the formation of metal silicide zones 5, 6 and 7, which are provided on, respectively, the gate, source and drain regions of the transistor.

The silicidation stage enables a less elevated resistance of the polysilicon track 2 to be obtained.

However, as shown in Figure 1, the silicide zone 5 contacting the polysilicon region 2 has a curved interface with this polysilicon region, which is caused by mechanical stresses induced during the chemical reaction between titanium and silicon.

Apart from the fact that said curved surface is less suitable for making contact, at a later stage, than a flat surface, the thickness of the silicide formed is smaller at certain locations, and it has been found that the bonding power obtained would cause a partial retreat of the silicide during subsequent process steps. Finally, this results in a smaller quantity of silicide, causing a smaller reduction of the resistance of the polysilicon track.

It is an object of the invention to overcome this problem.

The invention more particularly aims at improving the silicidation of the polysilicon tracks, thereby causing, in particular, the adhesion of the silicide to the silicon to be improved and hence a more efficacious reduction of the resistance of these polysilicon tracks.

The invention also aims at reducing the mechanical stresses induced in the polysilicon in the course of the silicidation process, thus enabling, in particular, a substantially flat upper silicide surface to be obtained.

This object is achieved in accordance with the invention by a method of manufacturing an integrated circuit, which method includes a stage wherein lateral isolation regions (spacers) are formed at the sides of at least one projecting polysilicon region so as to be in contact therewith, said lateral isolation regions each being composed of a smaller isolation layer, which is in contact with said projecting region, and of a larger isolation layer. The method also includes a silicidation process to which the upper part of the polysilicon region is subjected, which silicidation process includes the deposition on said upper part of a metal layer which is capable of forming a metal silicide with the silicon.

In accordance with a general characteristic of the invention, the silicidation process includes, prior to the deposition of said metal layer, an etch step to which at least the vertical portion of the smaller isolation layer is subjected so as to form a trench of predetermined depth between the larger isolation layer of each lateral isolation region and the corresponding side of the polysilicon layer. Moreover, the deposition of the metal layer, for example of titanium, is a directional deposition, which is carried out using, for example, a honeycomb-structured collimator, enabling the trenches thus obtained to be correctly filled.

In other words, an etch process carried out on the smaller isolation layer (at least the vertical portion thereof) so as to detach at least the upper part of the polysilicon layer is inherent in the invention, said etch process enabling the mechanical stresses developing in this upper part during the silicidation to be reduced. In addition, filling the trenches obtained by means of the directional metal deposition results in an improved lateral silicidation of the polysilicon region. Those skilled in the art will be capable of adjusting the

desired depth of the trenches as a function of, in particular, the dimensional characteristics of the polysilicon regions and the spacers in order to achieve the effect as desired by the invention, and taking into account the intended application.

In this case, it has been found that, in order to substantially improve the silicidation, the depth of the trenches preferably should be at least $1/20^{th}$ of the height of the projecting polysilicon region.

Those skilled in the art will also be capable of adjusting the depth of the trenches in such a way that the larger isolation layer (typically of silicon nitride) of the spacers does not become detached. In this respect, it has been found that a trench depth of maximally half the height of the larger isolation layer and maximally half the thickness of the larger isolation layer would reduce the risk of said larger isolation layer becoming detached.

The vertical portion of the smaller isolation layer of the spacers may be etched using an anisotropic etch process. In this case, only the vertical portion of the smaller isolation layer of the spacers is etched.

The vertical portion of the smaller isolation layer may alternatively be etched using an isotropic etch process. This results in the formation of a horizontal trench inside each spacer, which horizontal trench is made in the smaller isolation layer between the larger isolation layer and the substrate of the integrated circuit, said horizontal trench extending from the side edge of the larger isolation layer of the spacer. Such a horizontal trench enables a further reduction of the risk of short-circuits between the silicidized source and drain regions, on the one hand, and the silicidized gate region on the other hand.

The invention also aims at providing an integrated circuit comprising lateral isolation regions formed at the sides of at least one projecting region of polysilicon so as to be in contact therewith, each lateral isolation region being composed of a smaller isolation layer, contacting said projecting region, and a larger isolation layer. The integrated circuit further comprises a zone including a metal silicide situated in the upper part of the polysilicon region.

In accordance with a general characteristic of the invention, each lateral isolation region comprises a vertical trench made in the smaller isolation layer between the larger isolation layer and the corresponding side of the projecting region, said trench extending from the top of the larger isolation layer of the corresponding lateral isolation region down to a predetermined depth.

These and other objects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter.

In the drawings:

Fig 1, already described hereinabove, diagrammatically shows a transistor in accordance with the prior art, and

Figs. 2 through 8 diagrammatically show different steps in the implementation of the method in accordance with the invention; Fig. 8 more particularly shows a part of an integrated circuit in accordance with the invention.

In Fig. 2, reference numeral 1 denotes a semiconductor substrate of silicon, and reference numeral 70 denotes a lateral isolation zone, or field oxide, which is typically made of silicon dioxide, and which serves, for example, to isolate the active zone formed in the silicon substrate 1 from another active zone.

After the formation, in a customary manner, of a gate oxide layer 3, and after the deposition, in a customary manner, of a polysilicon layer and etching of the latter, polysilicon tracks 2 are obtained (shown in section in different planes), comprising, for example, a projecting region which is formed above the substrate and which serves to form the field-effect gate region of a transistor, and another projecting region which is formed above the field oxide and which serves to connect together two gate regions of two adjacent transistors.

The height of the projecting region of polysilicon 2 generally lies in the range between 1500 and 2500 Å, for example approximately 2000 Å.

Subsequently, a smaller isolation layer 400, typically of TEOS oxide, is similarly deposited in a manner which is known per se (Fig. 3), said smaller isolation layer having a thickness of the order of, for example, 200 Å. Next, a larger isolation layer 410, typically of silicon nitride, is similarly deposited in a manner which is also known per se.

After subjecting the larger isolation layer 410 to an anisotropic etch process, the configuration shown in Fig. 4 is obtained, wherein the etched, larger isolation layer 411is used to form the larger isolation layer of the spacers arranged so as to contact the vertical, lateral sides of the projecting regions of polysilicon.

It is to be noted that the smaller isolation layer 400 can be used as a stop layer in this anisotropic etch process.

Subsequently (see Fig. 5), a customary process is carried leading to a reduction of portions of the smaller isolation layer 401 obtained in Fig.4, which portions are situated on the polysilicon regions and outside the layer 411.

This results in the formation of spacers formed by the smaller isolation layer 402 and the larger isolation layer 411. The total thickness of the spacers generally lies in the

range between 50 nm and 100 nm, for example 70 nm. To be more precise, the thickness E of the larger isolation layer 411 is, for example, 50 nm while the thickness of the smaller isolation layer 402 is, for example, 20 nm.

After the customary doping operations of the drain and source regions have been carried out in the semiconductor substrate as well as the subsequent high-temperature annealing process at a temperature above, for example, 1000°C for 5 to 50 seconds, a layer 8 is deposited which is composed of a material which serves to protect a part of the integrated circuit against the subsequent silicidation step. This protection material may be silicon dioxide or TEOS oxide or TEOS oxide covered with silicon nitride.

Next (see Fig. 6), the material 8 is subjected to an etch treatment so as to remove it at the location of the region of the integrated circuit involved in the silicidation process.

If the material 8 is identical to the material used for the smaller isolation layer 402, then the etch treatment of the material 8 is extended so as to include an overetch treatment leading to the formation of a vertical trench TR having a predetermined depth h between the larger isolation region 411 of the spacers and the corresponding side F of the projecting polysilicon region.

If, however, the material 8 differs from the material of the smaller isolation layer 402 of the spacers, then an additional, selective etch treatment is carried out to form the trenches TR.

If the etch treatment of the material 8 and, possibly, the additional etch treatment are anisotropic etch treatments, then only the vertical portion of the smaller isolation layer 402 is etched. In this case, preferably, but not necessarily, one or more isotropic etch processes are carried out in order to form also horizontal trenches TH between the larger isolation layer 411 and the substrate 1, said trenches extending from the outer lateral edge of the larger isolation layer 411 of the spacers. The function and the usefulness of these horizontal trenches TH will be described hereinbelow.

The depth h of the vertical trenches TR is preferably at least equal to $1/20^{th}$ of the height H of the projecting polysilicon region, resulting in a substantial improvement of the silicidation by a reduction of the mechanical stresses in the polysilicon.

Moreover, in order to preclude that the larger isolation layer 411 of the spacers becomes detached, said depth h preferably remains below half the height H1 of the larger isolation layer 411, and also below half the thickness E of said layer 411.

This means, in a practical indication of the above ratios, that for a height H of the polysilicon of the order of 200 nm, a height h of the order of at least 10 nm leads to a substantial improvement of the silicidation.

It is to be noted that the presence of the oblique sides FO on the field oxide 70 is caused by oxide consumption during the manufacturing process.

When the trenches have been formed, a metal 9 (see Fig.7) which is capable of forming a metal silicide with the polysilicon is deposited. This is a directional deposition which is carried out using, for example, a honeycomb-structured collimator, so that the trenches TR can be filled, which would not be possible if use was made of a customary powder-coating process.

After the silicidation step, a first annealing step is carried out using equipment that is known per se, said annealing step being carried out a temperature in the range between 650°C and 800°C (for titanium) for a period of time ranging between 10 and 30 seconds, and a temperature of, for example 450°C for cobalt.

This first annealing process causes the titanium to be converted to titanium silicide $TiSi_2$, more particularly to a titanium silicide known to those skilled in the art as $TiSi_2$-C49. This formation of titanium silicide takes place through contact with the polysilicon as well as through contact with the silicon of the substrate.

Through contact with the larger isolation layer 411 of the spacers, titanium nitride TiN and titanium oxides TiO_x are formed. Titanium nitrides also form above the titanium silicide.

It is to be noted that the trenches TR, which have been filled with titanium at an earlier stage, improve the lateral silicidation of the polysilicon regions.

After the first annealing process, a selective reduction, which is known per se, of the titanium nitride, the titanium oxides TiO_x and the titanium is carried out. This selective reduction is obtained, for example, by wet-etching in a bath on the basis of ammonia and hydrogen peroxide (H_2O_2). It is to be noted that a small quantity of $TiSi_2$ is consumed in this wet-etching process.

Subsequently, a second high-temperature annealing process is carried out, typically at temperatures above 800°C, for example 900°C, for a few seconds, for example about ten seconds, in order to convert the titanium silicide C49 to a less resistive titanium silicide known to those skilled in the art as C54. Also in this case, the conversion takes place under more favorable conditions than in the method according to the prior art, which can be

attributed to the reduction of the mechanical stresses in the polysilicon, which reduction is attributable to the presence of vertical trenches.

After said annealing process, the configuration shown in Fig. 8 is obtained. In Fig. 8, reference numeral 5 denotes the metal silicide zone situated on the upper part of the projecting regions of silicon. Reference numerals 6 and 7 denote the metal silicide zones situated on the source and drain regions of the transistor. The upper surface of the metal silicide zone 5 is quasi planar. Furthermore, in the course of the annealing processes, particularly during the first annealing process, a small portion of the silicon is consumed. However, if said reduction in height is taken into account as well as the height of the metal silicide 5, a height H2 of the silicidized polysilicon region is obtained which is approximately equal to the initial height H of the polysilicon region.

Consequently, the height h of the vertical trenches TR remains preferably equal to at least $1/20^{th}$ of the height H2.

Furthermore, the selective reduction of the titanium oxides, the titanium nitride and, possibly, the unreacted titanium, carried out between the two annealing processes, may result in titanium nitride residues and/or titanium oxide residues being left behind on the surface of the larger isolation layer 411, which residues may cause short-circuits between the zones if they simultaneously contact the silicidized gate zones and the silicidized drain/source zones. This risk of short-circuits is minimized by the presence of the horizontal trenches TH

CLAIMS:

1. A method of manufacturing an integrated circuit, which method includes a stage wherein lateral isolation regions (spacers) are formed at the sides of a projecting polysilicon region so as to be in contact therewith, said lateral isolation regions each being composed of a smaller isolation layer (402), which is in contact with said projecting region (2), and of a larger isolation layer, which method also includes a silicidation process to which the upper part of the polysilicon region is subjected, which silicidation process includes the deposition on said upper part of a metal layer which is capable of forming a metal silicide (5) with the silicon, characterized in that the silicidation process includes, prior to the deposition of said metal layer, an etch step to which at least the vertical portion of the smaller isolation layer (402) is subjected so as to form a trench (TR) of predetermined depth (h) between the larger isolation layer (411) of each lateral isolation region and the corresponding side (F) of the polysilicon region (2), and in that the deposition of the metal layer is a directional deposition.

2. A method as claimed in claim 1, characterized in that the depth (h) of the trench is at least equal to $1/20^{th}$ of the height (H) of the projecting region.

3. A method as claimed in claim 1 or 2, characterized in that the depth (h) of the trench is equal to maximally half the height (H1) of the larger isolation layer and maximally half the thickness (E) of the larger isolation layer.

4. A method as claimed in any one of the preceding claims, characterized in that the vertical portion of the smaller isolation layer (402) is anisotropically etched.

5. A method as claimed in any one of the claims 1 to 3, characterized in that the vertical portion of the smaller isolation layer (402) is isotropically etched.

6. An integrated circuit comprising lateral isolation regions formed at the sides of at least one projecting region of polysilicon so as to be in contact therewith, each lateral

isolation region being composed of a smaller isolation layer (402), contacting said projecting region (2), and a larger isolation layer (411), and comprising a zone (5) including a metal silicide situated in the upper part of the polysilicon region (2), characterized in that each lateral isolation region comprises a vertical trench (TR) made in the smaller isolation layer (402) between the larger isolation layer (411) and the corresponding side (F) of the projecting region (2), said trench (TR) extending from the top of the larger isolation layer (411) of the corresponding lateral isolation region down to a predetermined depth (h).

7. An integrated circuit as claimed in claim 6, characterized in that the depth (h) of the trench (TR) is at least equal to $1/20^{th}$ of the height (H2) of the projecting region of silicidized polysilicon.

8. An integrated circuit as claimed in claim 6 or 7, characterized in that the depth (h) of the trench (TR) is equal to maximally half the height (H1) of the larger isolation layer and equal to maximally half the thickness(E) of the larger isolation layer.

9. An integrated circuit as claimed in any one of the claims 6 to 8, characterized in that each lateral isolation region comprises a horizontal trench (TH) made in the smaller isolation layer (402) between the larger isolation layer (411) and the substrate (1) of the integrated circuit, said trench extending from the lateral edge of the larger isolation layer of the lateral isolation region.

FIG.1

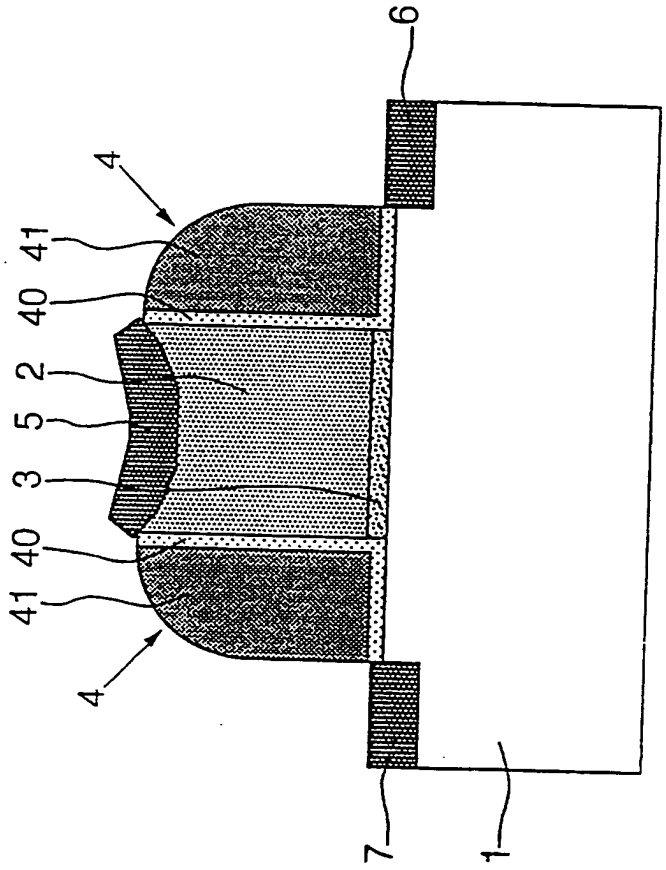


FIG.2

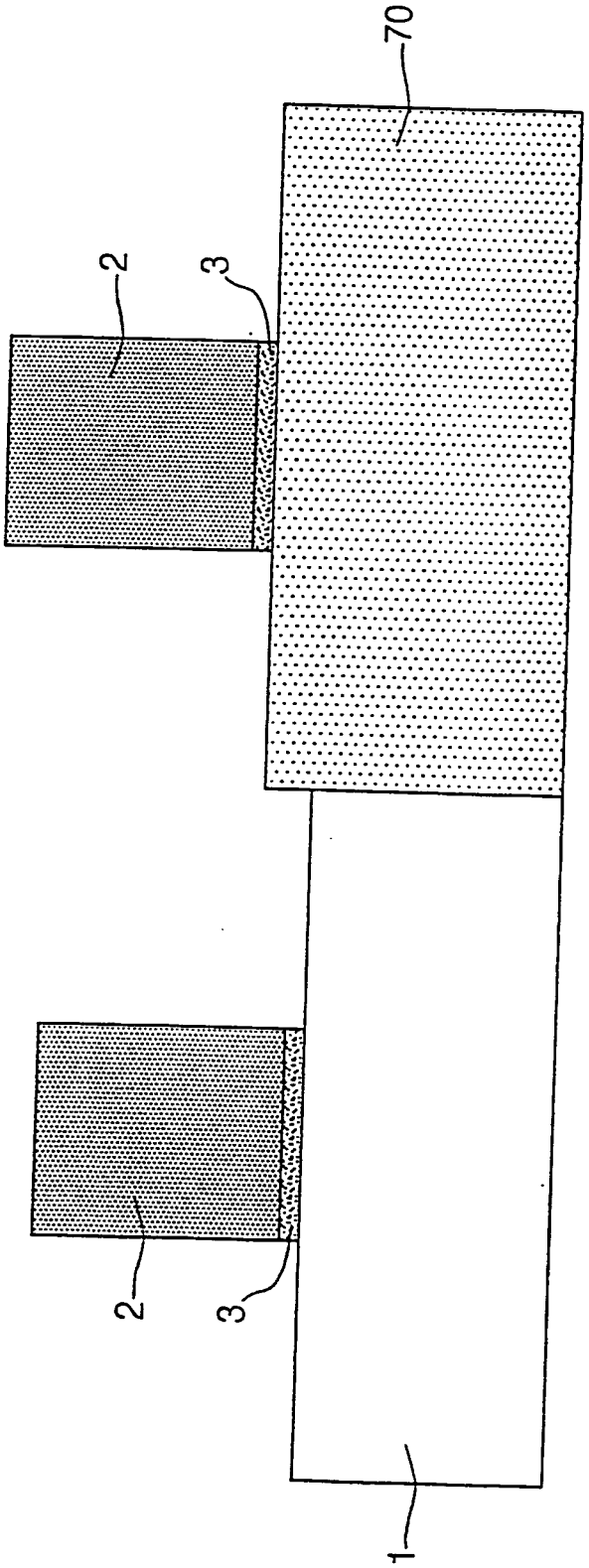


FIG.3

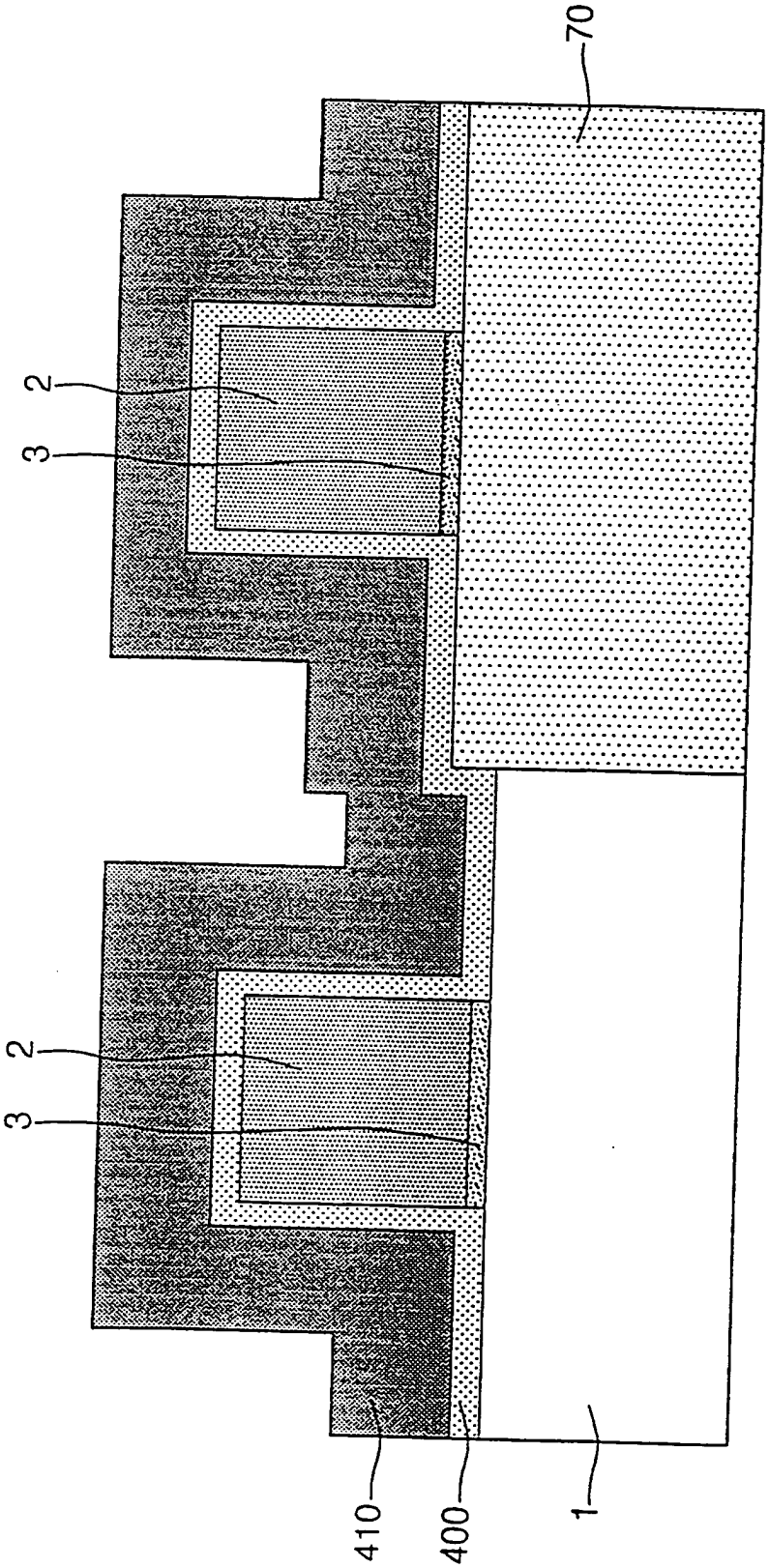


FIG.4

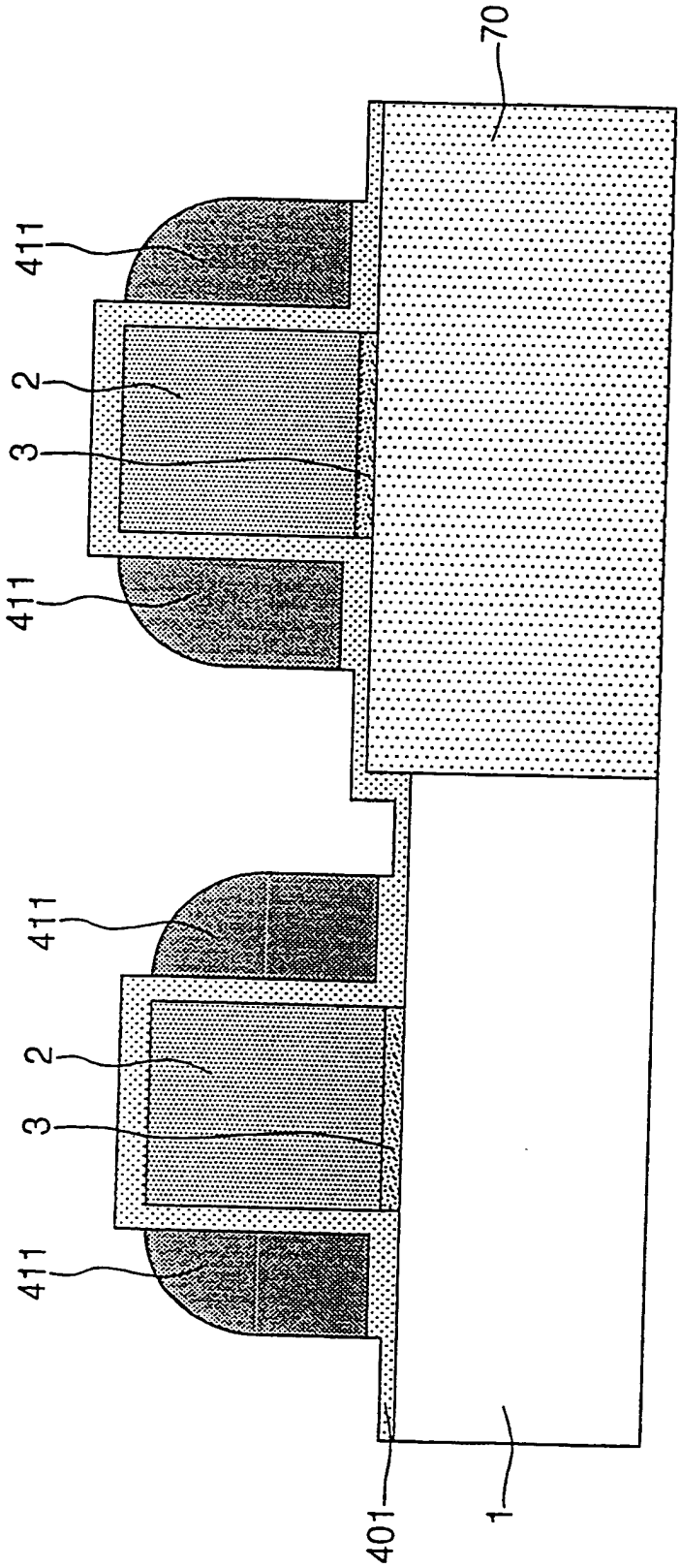


FIG.5

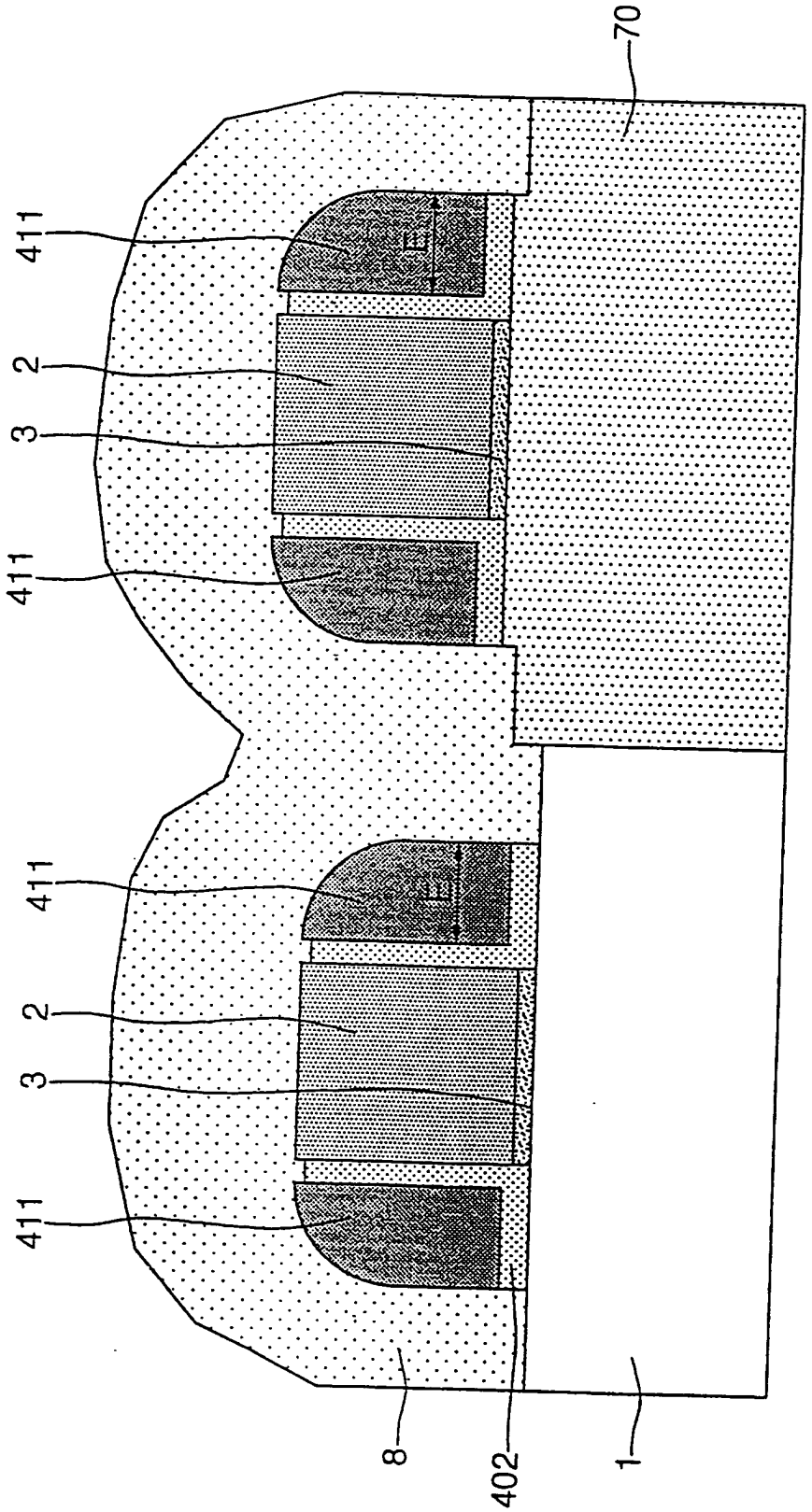


FIG.6

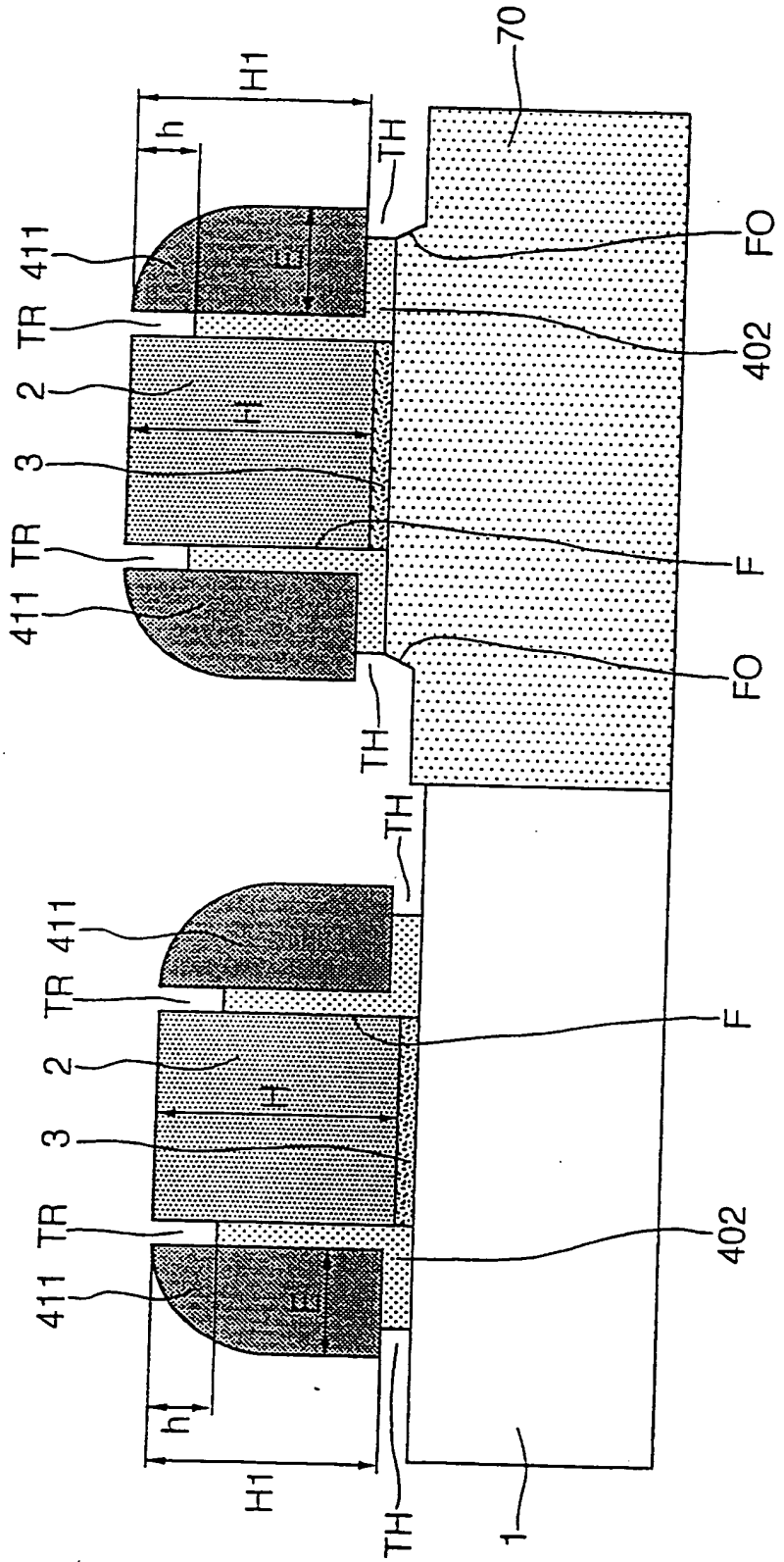

70
H1
h
TH
411
E1
FO
TR
402
2
H
3
F
411
TR
FO
TH
TH
411
TR
F
2
H
3
411
TR
402
E1
h
H1
TH
1

FIG.7

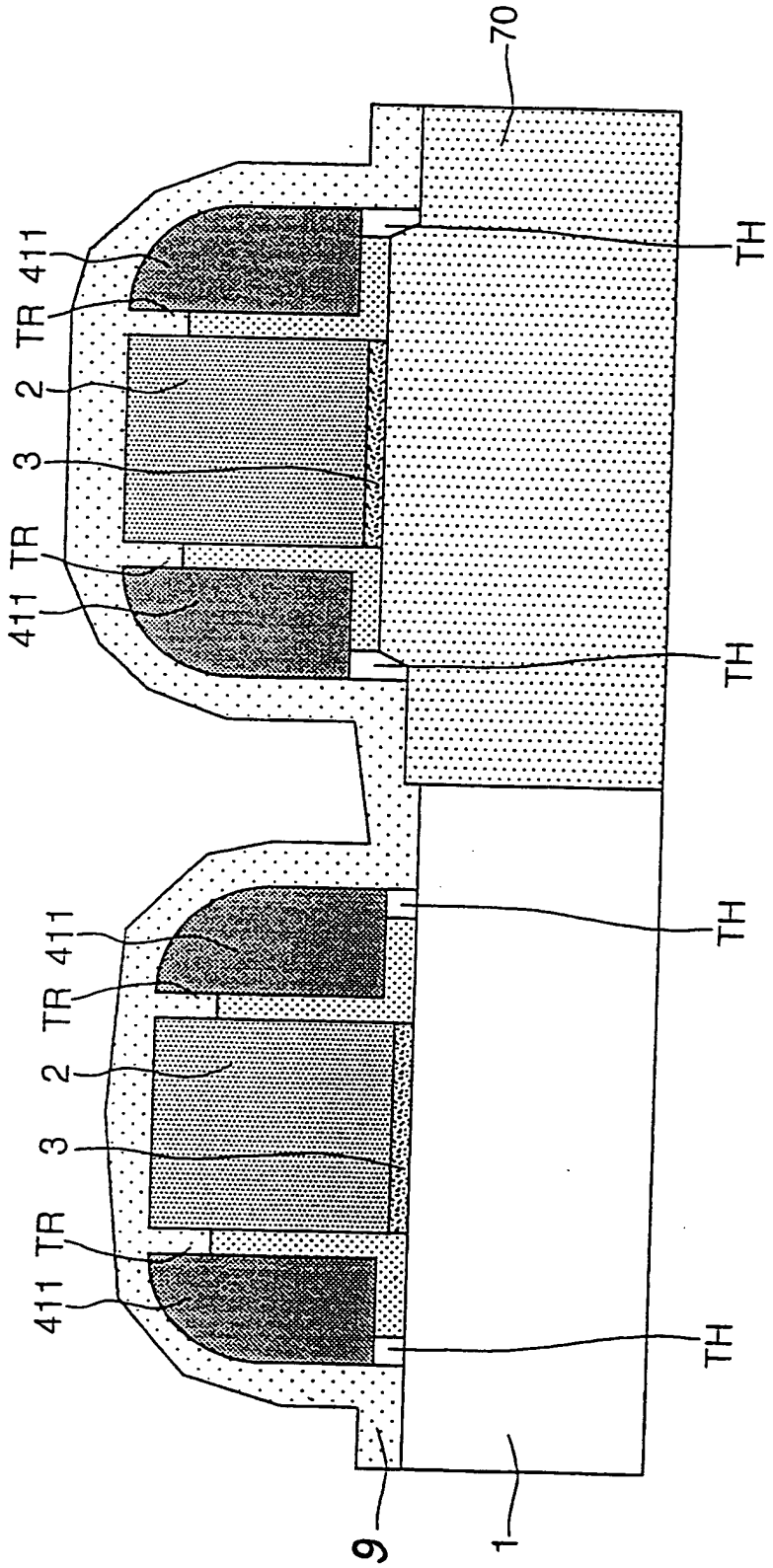
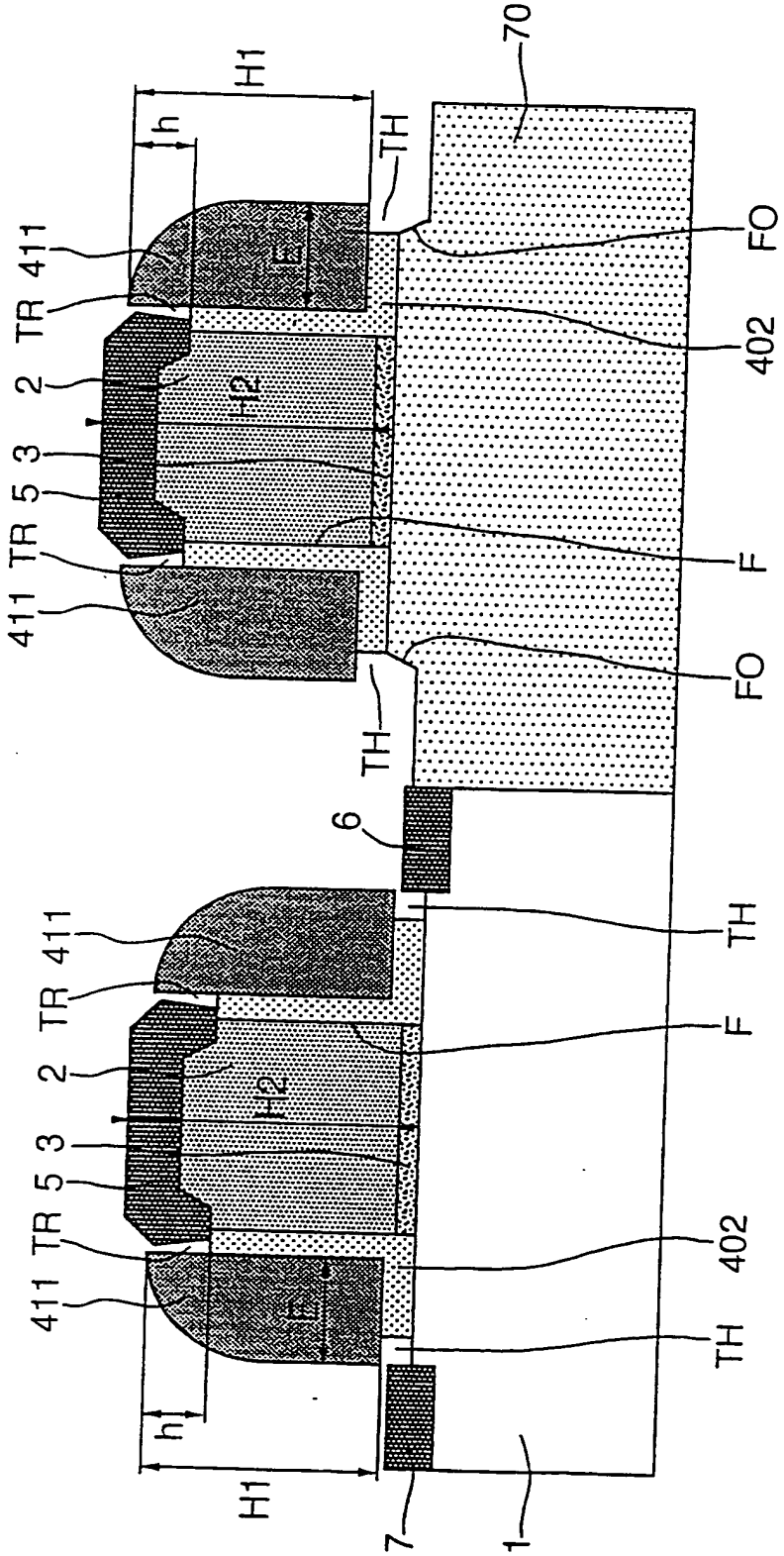


FIG.8



INTERNATIONAL SEARCH REPORT

[redacted] al Application No
[redacted] T/EP 00/07519

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/28 H01L21/8238

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5 739 573 A (KAWAGUCHI HIROSHI) 14 April 1998 (1998-04-14) column 10, line 5 -column 14, line 48; figures 5,6	1-4,6-8 5
Y	PATENT ABSTRACTS OF JAPAN vol. 1995, no. 06, 31 July 1995 (1995-07-31) -& JP 07 066406 A (OKI ELECTRIC IND CO LTD), 10 March 1995 (1995-03-10)	5
X	abstract; figure 1	6-9
X A	US 5 783 479 A (HUANG TIAO-YUAN ET AL) 21 July 1998 (1998-07-21) column 2, line 56 -column 3, line 54; figure 1	6-9 2-5

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 December 2000	12/12/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Gélébart, J

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

[redacted]tion on patent family members

[redacted]ial Application No
[redacted]/EP 00/07519

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5739573 A	14-04-1998	JP 2606143 B	30-04-1997
		JP 8037301 A	06-02-1996
		KR 195369 B	15-06-1999
JP 07066406 A	10-03-1995	NONE	
US 5783479 A	21-07-1998	NONE	